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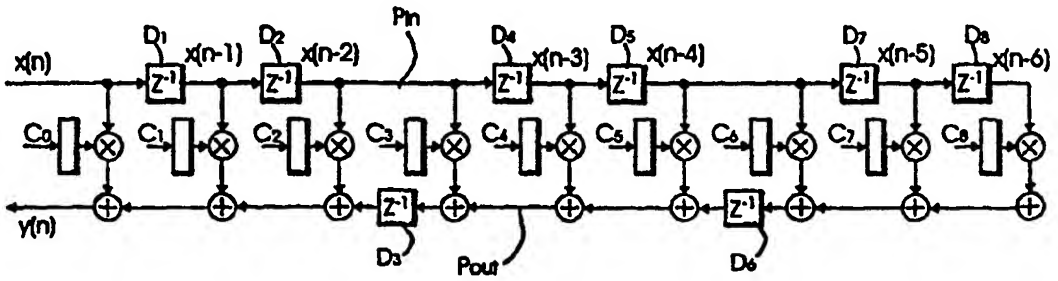
(54) Title: FIR FILTER STRUCTURE WITH LOW LATENCY FOR GIGABIT ETHERNET APPLICATIONS



(57) Abstract

A digital filter has an input path and an output path and includes a set of delay elements and a number of taps. The taps couple the input path to the output path. Each of the taps has a coefficient, a multiplier and an adder. Each of the delay elements is disposed between two adjacent taps. The delay elements are placed in either the input path and the output path of the digital filter, such that the digital filter has fewer delay elements in the input path than a direct-form digital filter with the same number of taps in a direct-form structure, and has fewer delay elements in the output path than a transposed-form digital filter with the same number of taps in a transposed-form structure; and such that the digital filter has same transfer function as the direct-form digital filter and the transposed-form digital filter.

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INTERNATIONAL SEARCH REPORT

Im .donal Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03H17/06 H04B3/23 H04B3/32 H04L25/14 H04L25/497 H04L1/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03H H04B H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DUNCAN ET AL.: "Strategies for design automation of high speed digital filters" JOURNAL OF VLSI SIGNAL PROCESSING, vol. 9, no. 1/2, September 1995 (1995-09), pages 105-118, XP000525889 Dordrecht, NL page 105, left-hand column, paragraph 1 page 105, right-hand column, paragraph 3 page 108, right-hand column, paragraph 2 - paragraph 4 page 108, right-hand column, paragraph 6 -page 109, left-hand column, paragraph 1 --- -/--	1-20

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
26 April 2000	09/05/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Scriven, P

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In. ational Application No
PCT/US 99/26483

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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X	PEKMESTZI, CARAISCOS: "Implementation of systolic multipliers and digital filters via signal flow-graph transformations" THE MEDITERRANEAN ELECTROTECHNICAL CONFERENCE, 12 - 14 April 1994, pages 105-108, XP000506110 New York, US ISBN: 0-7803-1773-4 page 107, left-hand column, paragraph 1 ---	1-20
A	WO 98 43369 A (LEVEL ONE COMMUNICATIONS) 1 October 1998 (1998-10-01) page 7, line 25 - line 28 -----	1,11

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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PCT/US 99/26483

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WO 9843369 A	01-10-1998	AU 6773698 A	20-10-1998
		EP 0972356 A	19-01-2000